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PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10077258	FILING DATE 02/14/2002	CLASS 257	SUBCLASS 324	GAU 2814	EXAMINER <i>[Signature]</i>
<b>**APPLICANTS:</b> Mo Brian; Chau Duc; <i>yft</i>					
<b>**CONTINUING DATA VERIFIED:</b> <i>yel</i> THIS APPLICATION IS A DIV OF 09/286,168 04/05/1999 <i>yft</i>					
<b>BEST AVAILABLE COPY</b>					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> <i>none yft</i>					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>			RESCIND <input type="checkbox"/>		
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no			ATTORNEY DOCKET NO		
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no			018865-001010US		
Verified and Acknowledged Examiners's initials <i>yft</i>					
TITLE : Method of forming a trench transistor having a superior gate dielectric U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)					

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims 10	Print Claim for O.G. 1
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg. 5	Figs. Drwg. 7
		Print Fig. 3, 4	
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		Primary Examiner	
		<b>PREPARED FOR ISSUE</b>	
		Application Examiner	
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